Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **ANODE**
2. **CATHODE**
3. **N/C**
4. **N/C**
5. **N/C**
6. **N/C**
7. **N/C**

**.032”**

**1**

**7**

**4**

**7 6 5**

**3**

**.032”**

**Top Material: Al**

**Backside Material: Bare Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: FLOATING**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .032” X .032” DATE: 6/1/23**

**MFG: SILICON SUPPLIES THICKNESS .011” P/N: LM4040A1-4.1**

**DG 10.1.2**

#### Rev B, 7/1